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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/605,408	Confirmation No. **2407**
Applicant	:	Kern Rim	
Filed:	:	September 29, 2003	
TC/Art Unit:	:	2813	
Examiner	:	James M. Mitchell	
Docket No.	:	YOR920000707US2	
Customer No.	:	27127	

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

DECLARATION UNDER 37 CFR §1.131

I, Kern Rim, depose and say that:

(1) I am the sole inventor of the subject matter covered by each of the claims pending in the above-identified U.S. patent application (the "Application").

(2) I am currently employed with International Business Machines Corp. (IBM), the assignee of the Application.

(3) Prior to February 7, 2002, I conceived and completed, in this country, my disclosed and claimed invention for a method of forming a strained silicon-on-insulator (SSOI) structure involving the steps of: forming a silicon layer on a strain-inducing layer with a different lattice constant than silicon so that the silicon layer is strained; bonding the resulting multilayer

structure to a substrate so that an insulating layer is between the strained silicon layer and the substrate; and then removing the strain-inducing layer to yield a strained silicon-on-insulator structure comprising the substrate, the insulating layer on the substrate, and the strained silicon layer on the insulating layer. Completion of this method is evidenced attached hereto as Exhibits A through G, each of which are documents in existence prior to February 7, 2002.

(4) Exhibit A is a split table detailing eight "wafer types" to be prepared according to the method recited in claims of the Application.

(5) Exhibit B is an email in which I requested 20% SiGe wafers identified in the table of Exhibit A.

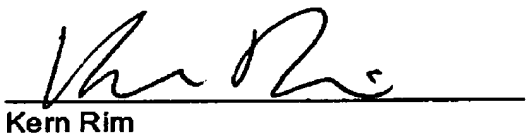
(6) Exhibit C is an email confirming receipt of the wafers requested in Exhibit B and discussing an experiment underway on the wafers. At this point the success of the process was uncertain, as evident from this email.

(7) Exhibit D is an email reporting progress in the experiment and requesting assistance in removing the strain-inducing SiGe layer from the experimental wafers.

(8) Exhibit E is an email which expresses anticipated good results when the experiment is completed within a period prior to February 7, 2002.

(9) Exhibit F is an email discussing carrying out the final step of etching to remove the SiGe layer of the SSOI wafers already processed in the experiment. This final step was successfully completed prior to February 7, 2002.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.



Kern Rim

Exhibit A

	A	B	C	D	E	F
1	SSSTI1					
2						
3	Wf#	Wafer ID	Wafer Type	Wafer Note	Description	Description
4	1	M918E9F	20%	20SS006 350A	SSOI	
5	2	ME18CNF	20%	20SS006 350A	SSOI	
6	3	M018WAF	15%	15SS002 350A	SSOI	
7	4	MX18WBF	15%	15SS002 350A	SSOI	
8	5	MZ18BLF	A 20% SiGe + 500A Si	DSGOI02	Control thin SOI	
9	6	M9188VF	A 20% SiGe + 500A Si	DSGOI02	Control thin SOI	
10	7	M2187KF	A 20% SiGe + 500A Si	DSGOI02	Control thin SOI	
11	8	M7187FF	A 20% SiGe + 500A Si	DSGOI02	Control thin SOI	

Experiment Split Table from [redacted]

File name: SSOI1.123

Exhibit B

Ken Rim/Watson/IBM To Jack O Chu
cc
bcc
Subject wafers

Jack,

I would like to release Center 1 device lot next week. How is the wafer situation these days? I'd need 5 15% and 5 20% wafers.

Other wafer needs that are imminent:

SSOI experiment: 4 with ~500 A pseudomorphic SiGe 20%
2~3 SiGe buffer wafers (Si cap does not matter) for CMP practice (don't have to be device grade)

Ron's silicide experiemnt.

I'll give you a call when I get back tomorrow. Thanks!

Ken

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Exhibit C

Ken Rim/Watson/IBM

[redacted]

To Erin C Jones/Watson/IBM@IBMUS
cc Meikei leong/Fishkill/IBM@IBMUS
bcc
Subject *IBM Confidential: ssoi experiment

Erin,

Remember that crazy idea I talked to you about back in fall? Transferring strained Si right on insulator?

I finally got a few wafers from Jack and gave them to Leathen. (We had the supertrk run sheet written a while ago.) The goal of this experiment is simply to check if the transferred layer can retain any of the strain. If any of the strain is indeed retained, we will want to do some annealing experiments, and I am hoping your group (Kevin, new hire, etc.) and Jack can help with taking the idea further. It's essentially very similar to what is know as "Ultra-Cut", and should be interesting just a way to create a thin, uniform SOI even if it is not strained.

I think it is a risky experiment in terms of rate of success, but if it works, I think this could be something we can consider for beyond 11S.

Just thought I would let you know in case you have any concerns or objections. Right now, I wanted to keep it as a very low key low profile experiment, mostly because it might turn out to be a bad idea!

Ken

[redacted]

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Exhibit D

Ken Rim/Watson/IBM

To Jack O Chu/Watson/IBM@IBMUS

cc Leathen Shi/Watson/IBM@IBMUS

bcc

Subject SSOI experiment

Jack,

Leathen finished bonding, grinding back, and CMP on the strained Si-directly-on-insulator. He has 6 (I think) wafers. A couple of them are control wafers with Si/pseudomorphic SiGe stacks.

The next steps were going to be thicness measurement by nanospec, litho patterning to put some patterns for easy step height measurement, and careful selective etch of SiGe. Since I've been busy, I've been just waiting for the right moment to do this.

When you mentioned the SSOI at today's meeting, I just remembered. Since you have some experience with HHA etch, and since you may have some time now while your reactor is down, if you want to join this experiment, maybe you can help with the etch back? I was going to first do some etch rate test on blanket SiGe wafers, and then break up one of the wafers to try the etch back on pieces

Let me know if you are interested.

Thanks.

Ken

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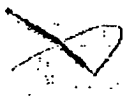
Exhibit E



Jack O Chu/Watson/IBM
[redacted]

To: Ken Rim/Watson/IBM@IBMUS, Erin C Jones/Watson/IBM@IBMUS, Meikei Ieong/Fishkill/IBM@IBMUS, Kevin K Chan/Watson/IBM@IBMUS, Suri Hegde/Watson/IBM@IBMUS, Leathen Shi/Watson/IBM@IBMUS
cc: Alfred Grill/Watson/IBM@IBMUS, H-S Philip Wong/Watson/IBM@IBMUS
bcc:
Subject: *IBM Confidential: SSOI and SGOI

- Ken,

I've already started a couple of runs with Leathen for making t-SGOI & SSOI and hopefully in the next month or so, I'll have some "good" results.

- - Jack

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---------- Forwarded by Jack O Chu/Watson/IBM on 10/25/2001 02:16 PM ----------

Ken Rim
[redacted]

To: Erin C Jones/Watson/IBM@IBMUS, Kevin K Chan/Watson/IBM@IBMUS, Suri Hegde/Watson/IBM@IBMUS, Leathen Shi/Watson/IBM@IBMUS, Jack O Chu/Watson/IBM@IBMUS
cc: Meikei Ieong/Fishkill/IBM@IBMUS

From: Ken Rim/Watson/IBM@IBMUS
Subject: *IBM Confidential: SSOI and SGOI

Exhibit F

Ken Rim/Watson/IBM

To Jack O Chu/Watson/IBM@IBMUS

cc Alfred Grill/Watson/IBM@IBMUS, Erin C Jones/Watson/IBM@IBMUS, Kevin K Chan/Watson/IBM@IBMUS, Leathen Shi/Watson/IBM@IBMUS, Meikei Ieong/Fishkill/IBM@IBMUS, Suri Hegde/Watson/IBM@IBMUS

bcc

Subject Re: "IBM Confidential: SSOI and SGOI

Jack,

How far are you along with the process? Leathen bonded a few SSOI wafers (wafers you grew) for me (just SSOI, not SGOI) back last winter, and they have been just waiting for the HHA etching experiments. So they are already etched back down to the SiGe layer, and I just never had time to do the next steps- iterations to etch SiGe and stop on Si. I was going to ask Suri to help us drive this experiment and start a new batch with a couple of other ideas. Can we work with you, especially on these few wafers that are all ready for the last step, to get the HHA etch to work?

Ken

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